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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,934	03/06/2002	Amir Alon	IL920020007US1	7058

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EXAMINER
LEVIN, NAUM B

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,934	ALON ET AL.	
	Examiner	Art Unit	
	Naum B Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 10, 29 and 30 are objected to because of the following informalities:

Claim 10, line 1 "said sum of said currents" should be changed to -- a sum of currents --.

Claim 29, line 1 "said models" should be changed to -- a models --.

Claim 30, line 1 "said chip" should be changed to -- a chip --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-13, 15-21, 23-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Dansky et al. (US Patent 6,342,823).

Dansky discloses system and method for reducing calculation complexity of lossy, frequency-dependent transmission-line computation including:

(1), (16), (18), (24), (25), (26) A system for integrated circuit design comprising:

a high level design comprising a chip architecture, a floor plan, and one or more critical interconnect wire topologies (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

a schematic design comprising one or more circuit components and one or more critical interconnect wire models (col.5, ll.22-24 and ll.34-35);

a physical layout comprising said one or more circuit components and said one or more critical interconnect wire topologies (col.5, ll.19-24);

extracted parameters of said one or more circuit components and calculated parameters of said critical interconnect wire models (col.2, ll.20-33; col.3, ll.49-67 and col.4, ll.55-57); and

results of a simulation of a schematic design comprising said extracted parameters and said calculated parameters (col.2, ll.41-49 and col.4, ll.55-57);

(2) An integrated circuit design kit comprising:

one or more circuit components topologies (col.5, ll.19-24); and

one or more critical interconnect lines topologies (col.5, ll.19-24);

(3), (7), (23) The kit of claim 2 wherein said interconnect line topologies are predefined (col.5, ll.21-31);

(4) The kit of claim 2 and further comprising one or more circuit components models (col.5, ll.22-24 and ll.34-35);

(5) The kit of claim 2 and further comprising one or more critical interconnect lines models (col.5, ll.22-24 and ll.34-35);

(6) A topology of critical interconnect lines (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(8) The topology of claim 6 comprising a definite current return path (col.3, ll.34-37 and col.4, ll.31-36);

(9), (27) The topology of claim 6 wherein said topology is supplemented by a model comprising one or more of said following electrical parameters: capacitance, low frequency inductance, high frequency inductance, low frequency series resistance, high frequency series resistance, TEM impedance, and matrix representations of one or more of said parameters (col.2, ll.26-34 and col.3, ll.54-60);

(10) The topology of claim 6 wherein said sum of said currents of a cross section of said topology is zero (col.1, ll.32-33; col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(11) The topology of claim 6 wherein said topology comprises one or more signal wires and one or more shielding wires (col.2, ll.56-63);

(12) The topology of claim 11 wherein said one or more shielding wires is one or more side shielding wires located on one or more sides of said signal wires (col.3, ll.26-47);

(13) The topology of claim 11 and wherein said one or more shielding wires is a bottom shielding wire (col.3, ll.26-47);

(15) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a topology of critical interconnect lines (col.2, ll.36-49; col.3, ll.26-48; col.5, ll.22-24; col.6, ll.64-67 and col.8, ll.1-5);

(17) A computer software product for designing an integrated circuit, said product comprising a computer readable medium in which program instruction are stored, which instructions, when read by a computer, cause said computer to create a design kit comprising a topology of critical interconnect lines (col.2, ll.36-49; col.3, ll.26-48; col.5, ll.19-24; col.6, ll.64-67 and col.8, ll.1-5);

(19) A method for designing integrated circuits (IC), said method comprising the steps of:

(a) defining a chip architecture and a floor plan (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67);

(b) identifying one or more critical interconnect lines, and defining transmission line topologies for design of said critical interconnect lines (col.5, ll.21-31 and col.6, ll.64-67);

(c) determining a schematic design of said IC (col.5, ll.22-24 and ll.34-35);

(d) defining a physical layout of said IC (col.5, ll.19-24);

(e) extracting electrical parameters of said layout (col.2, ll.20-33; col.3, ll.49-67 and col.4, ll.55-57);

(f) simulating said schematic design (col.5, ll.40-41 and ll.48-51); and

(g) receiving results of said simulation (col.2, ll.41-49 and col.4, ll.55-57);

(20) The method of claim 19 and further comprising: (h) comparing said simulation results to a set of initial design requirements (col.5, ll.52-54);

(21) The method of claim 20 and further comprising: according to results of said step (h), repeating steps (d) to (g) (Fig.10);

(28) The method according to claim 19, wherein step (b) comprises: using one or more of said following to identify said critical interconnect lines: estimated length, metal level assignment and manual user selection (col.1, ll.17-19 and col.5, ll.21-31);

(30) A method for designing integrated circuits wherein defining said chip architecture and a floor plan comprises defining critical interconnect wires (col.3, ll.26-48; col.5, ll.22-24 and col.6, ll.64-67).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dansky.

With respect to claim 14 Dansky teaches the features above (for example col.2, ll.56-63 and col.3, ll.26-47) but lacks a system and method for IC design, where shielding wires may generate one or more shielding layers, witch is well known to a person of ordinary skills in the art at the time the invention was made.

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Dansky's teaching regarding the method and system using shielding layers to improve shielding effect in case of need.

6. Claims 22 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dansky in view of Segal (US Patent 6,496,972).

With respect to claims 22 and 29 Dansky teaches the features above but lacks a system and method for IC design, where IC is application specific integrated circuit (ASIC), and method further comprising creating parameterized cells from the models.

Segal discloses method and system for circuit design top level and block optimization including:

(22) The method of claim 19, wherein said integrated circuits are analog and mixed signal (AMS) circuits or application specific integrated circuits (ASIC) (col.1, ll.25-33);

(29) The method according to claim 19, and further comprising creating parameterized cells from said models (col.1, ll.63-67 and col.2, ll.1-27 and ll.54-62).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Segal's teaching regarding the system and method for IC design, where IC is application specific integrated circuit (ASIC), and method further comprising creating parameterized cells from the models and use it in Dansky's invention to improve an efficiency of implementing the integrated circuits design.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 703-305-0144. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

N L NL
March 27, 2003

A.M. Thompson
Patent Examiner
Technology Center 2800